

Photovoltaic Module-Integrated Stand-alone Single-Stage Switched Capacitor Inverter with Maximum Power Point Tracking

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Abstract—A switched capacitor (SC) based inverter that tracks the maximum power point (MPP) of a photovoltaic (PV) source and generates a pure sine output is presented. To enable integration with the PV module, efficiency and compactness are maximized with a single-stage topology that tracks the MPP of the PV source, boosts the input dc voltage, and generates a regulated ac output in a stand-alone configuration with scope for grid-connected applications. The SC inverter is realized with multiple identical SC blocks controlled by sinusoidal pulsewidth modulation and load-dependent output capacitor adjustment. A detailed steady-state analysis is carried out, and a mathematical model is derived to understand the interdependence of various inverter parameters on each other and to optimally choose the inverter components. A hardware prototype of the stand-alone single-stage SC inverter that operates from a 60 V/70 W PV module and delivers a 110 Vrms, 50 Hz output is wired to demonstrate the functioning of the proposed MPP tracking inverter under different operating conditions. An inversion efficiency $> 95\%$, a tracking efficiency $> 97\%$, and a total harmonic distortion (THD) $< 4\%$ have been practically achieved. All the details of this work are presented.

Index Terms—Inverter, maximum power point (MPP) tracking, module integrated, photovoltaic (PV) source, switched capacitor (SC).

I. INTRODUCTION

SWITCHED-capacitor (SC) power conditioners achieve power conversion by electronically switching capacitors between the input power source and the load. SC power conditioners are extensively used for dc–dc conversions. A lot of literature dealing with analysis [1], control methods [2], topologies [3], efficiency issues [4], and applications of SC dc–dc converters are available. The most distinguishing feature of SC dc–dc converters is the absence of inductors and transformers for handling power, leading to higher power densities compared to conventional dc–dc converters [5], [6]. The other relative advantages of SC dc–dc converters are efficiency over 95% under certain operating conditions [7] for a wide range of load variation, amenability for mass production and cost effectiveness, ruggedness and compactness due to the absence of magnetic components, easy thermal management

by heat steering techniques [4], and a wide spectrum of output power, ranging from a few milliwatts for single-chip power solutions [8] to over a kilowatt of output power [6].

SC power conditioners are not restricted only to dc–dc applications. SC power conditioners have been used for dc–ac, ac–ac [9], and ac–dc [10] conversions also. However, compared to SC dc–dc converters, the use of SC power conditioners for these applications has been relatively less explored.

Since this paper deals with SC dc–ac inverters, we now survey the literature available in this field. Reference [11] discusses a 24-W output SC-based dc–ac inverter. The input is 12 Vdc, and the output is 110 Vrms, 50 Hz sinusoidal output with 64 steps. The topology has two SC subcircuits, each containing 15 basic SC cells where each cell is composed of a capacitor, two MOSFETs, and two diodes. Chang has introduced two types of SC boost inverters in [12] and [13]. The one in [13] has n stages of SC voltage doublers for boosting the voltage to 2^n times the dc source voltage. It is followed by an H-bridge for generating ac output. The topology in [12] requires two equal dc voltage sources of opposite polarities to generate each half of the output sine wave. A total of $2(n - 1)$ SC cells are required for realizing an n -level sinusoidal output. Zou *et al.*, have analyzed a modular SC cell-based inverter topology powered from a dc source in [14]. Two types of SC cells are discussed. One is the full cell that can be used for dc–ac inversion, and the other is the half-cell that can perform both dc–dc and dc–ac operations. To realize a $2n + 1$ -level inverter, n full cells are required. An SC transformer is used in [15] and [16] to invert a dc input V_S to a sine output. The scheme in [15] gives a bucked sine output, whereas the one in [16] gives a boosted output. A five-level high-voltage SC inverter powered from a battery for driving the capacitive loads of electroluminescent displays is described in [17]. Ye *et al.*, describe an SC step-up multilevel inverter in [18]. It is a combination of a multilevel dc–dc converter and an H-bridge for unfolding. The inverter provides $2n + 3$ levels on the output voltage using n capacitors and $n + 5$ switches. An SC multilevel inverter consisting of an SC front-end stage powered from a 12 Vdc source followed by an H-bridge is used in [19] for high-frequency ac power distribution. A multilevel boost-type SC inverter powered from an 8 Vdc source for an inductive load is explained in [20]. All the SC inverters mentioned earlier are powered from constant dc voltage sources such as batteries.

Global efforts are on to reduce the cost of photovoltaic (PV) power production to $\$1 \text{ W}^{-1}$. Lowering the cost of the associated

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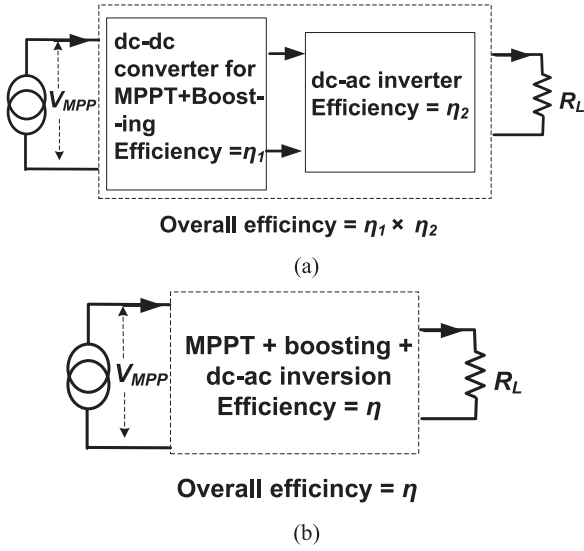


Fig. 1. Comparison of (a) two-stage and (b) single-stage solutions for MPP tracking, boosting, and inversion.

power electronics from $\$0.22 \text{ W}^{-1}$ to about $\$0.1 \text{ W}^{-1}$ is also part of this effort [21], [22]. Integrating the power electronics with the PV module is a step toward economization. SC power conditioners are excellent candidates for integration with PV sources compared to conventional power conditioners due their relative advantages such as compactness, ruggedness, ease of mass production, cost effectiveness, efficiency, etc. Hence, in this paper, we propose MPP tracking SC inverters for PV module integration.

Existing literature related to the use of SC power conditioners, in conjunction with PV sources, is surveyed. References [23] and [24] are some of the early attempts that have studied the feasibility to use SC dc-dc converters for tracking the maximum power point (MPP) of PV sources. SC converter based voltage equalization and current equalization methods are explored in [25] and [26], respectively, for mitigating the problems of module mismatch in series-connected PV modules. An SC power converter capable of performing MPP tracking of individual PV modules such that only the mismatch power between the PV modules is processed while converging each of the modules to their MPP is proposed in [27]. Scott *et al.*, [28] have presented an SC-based two-stage PV-module-integrated inverter. The first stage is an SC-based dc-dc converter that quadruples the input voltage, while the cascaded second stage is a five-level inverter that also does the MPP tracking. The transformerless SC-based topology investigated in [29] is a PV source fed grid-connected solution without voltage boosting capability, while the one in [30] is a two-stage boost topology with a grid interface.

Processing power from a PV source to get an ac voltage involves the following: 1) MPP tracking; 2) voltage boosting since the PV module voltage is usually lower than the required ac voltage; and 3) dc to ac inversion. This is usually achieved in two stages, as shown in Fig. 1(a), with an overall efficiency of $\eta_1 \times \eta_2$. Accomplishing this with a single stage is not only more efficient but also cost effective due to lower component count, as shown in Fig. 1(b). The SC-converter-based schemes

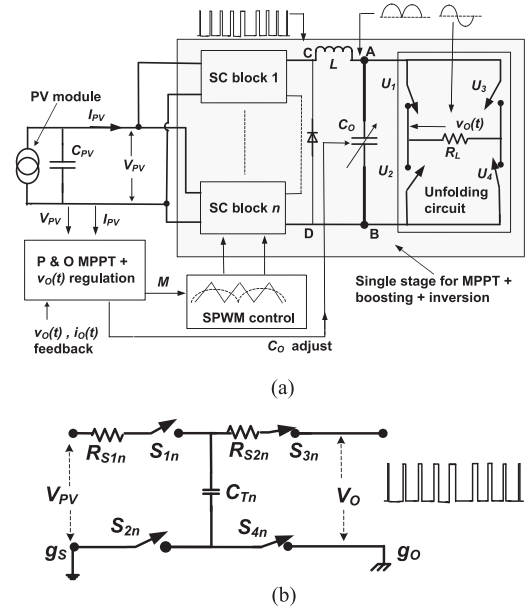


Fig. 2. PV-module-integrated single-stage SC inverter: (a) overall configuration and (b) n th basic SC building block of the inverter.

available till date for this [28], [30] and many of the proposals with conventional converters are two-staged solutions. Jain and Agarwal [31] have surveyed the single-stage solutions with conventional converters. Due to the obvious advantages of single-stage topologies, we propose a PV-module-integrated single-stage SC-based topology that tracks the MPP as well as boosts and inverts the PV source voltage ($\approx 60 \text{ V}$) to 110 Vrms , 50 Hz ac voltage. Most of the schemes available in literature are grid-connected systems. Unlike these, the scheme introduced in this paper is a stand-alone system, which can support loads directly connected to its output. However, it may be modified for grid-connected applications also. To the best of the authors' knowledge, a single-stage, boost-type, stand-alone solar PV inverter based on SC converters has not been reported so far in the literature.

II. PROPOSED TOPOLOGY

This section presents the block diagram of the proposed SC-based inverter, the process of dc to ac inversion and MPP tracking, and the algorithm for stand-alone operation.

A. DC-AC Conversion, SPWM, and MPP Tracking

The overall schematic of the SC-based PV-module-integrated single-stage boost MPP tracker and inverter is given in Fig. 2(a). The SC block that forms the basic building block of the inverter is shown in Fig. 2(b). This is a buck topology since a steady dc voltage $V_o < V_{PV}$ can be obtained by connecting an output filter capacitor [4]. In the absence of the output filter capacitor, voltage pulses as shown in Fig. 2(b) are obtained at the output. When S_{1n} and S_{2n} close, C_{Tn} charges. Then there is a dead time when all switches are open. Next, S_{3n} and S_{4n} close. Now, C_{Tn} discharges into the load. Thus, this topology generates a floating output voltage with respect to the source V_{PV} . By connecting the inputs of multiple basic SC blocks in parallel across the input

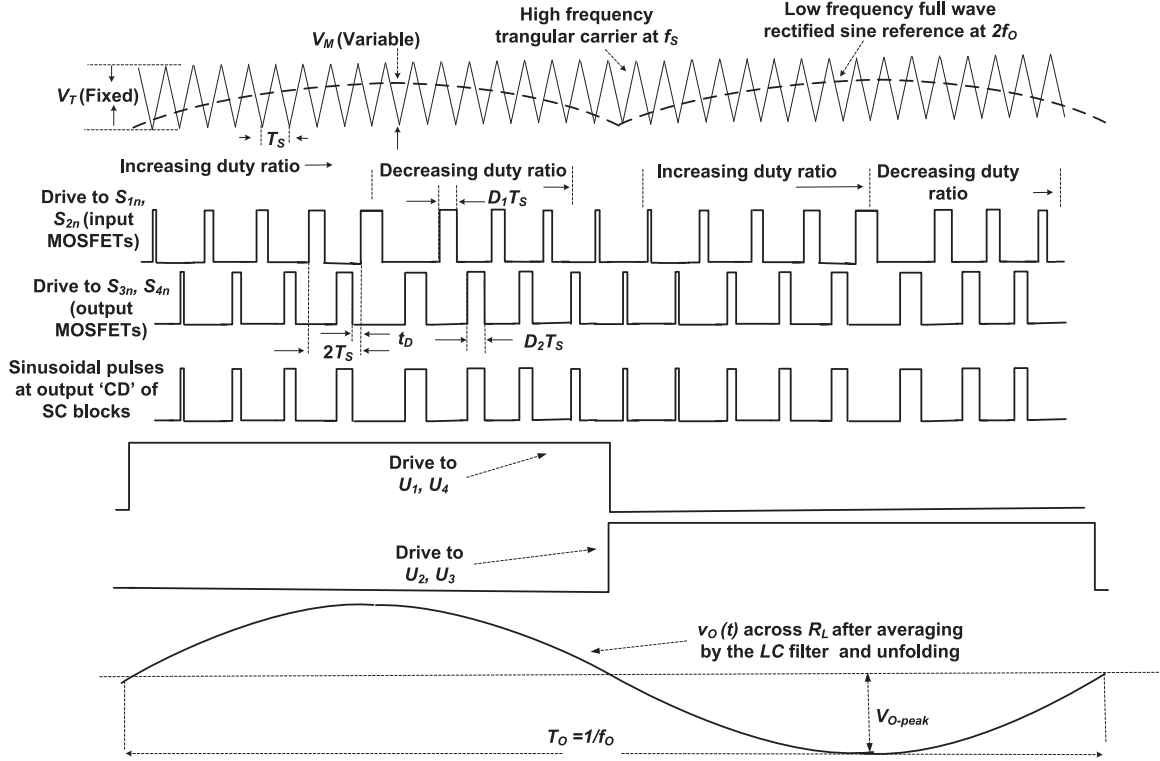


Fig. 3. SPWM for generating a sine output by comparing a high-frequency triangular carrier with a low-frequency full-wave-rectified sine reference.

source V_{PV} and their floating outputs in series, the topology can be used as a buck or boost, depending on the duty ratio (D_1 and D_2) of the switches. When the duty ratio is low, such a topology acts like a buck topology, and as the duty ratio increases, the topology acts like a boost topology.

Sinusoidal pulsewidth modulation (SPWM) is used due to its simplicity and ease of implementation. To minimize the distortion during zero crossing of $v_o(t)$ (crossover distortion), the output capacitor C_O is altered for different ranges of output load. This is explained in Sections V and VI.

Fig. 3 shows the generation of SPWM drive signals for the SC inverter by a single SPWM generator. It involves the comparison of a low-frequency full-wave-rectified sine reference of peak amplitude V_M at frequency $2f_o$ [where f_o is the frequency of $v_o(t)$], with a high-frequency triangular carrier of fixed peak amplitude V_T at frequency f_s . Let $1 \leq N \leq f_s/f_o$. Since $f_s \gg f_o$ (see Fig. 3), the ON duration $D_1 T_s$ of the input switches (S_{1n} and S_{2n}) of all the n SC blocks and the ON duration $D_2 T_s$ of the output switches (S_{3n} and S_{4n}) of all the n blocks are almost equal, i.e., $D_1 T_s \approx D_2 T_s$, where D_1 and D_2 generated by SPWM are given by

$$D_1 \approx D_2 = M |\sin(2\pi f_o N T_s)|; \quad M = \frac{V_M}{V_T}. \quad (1)$$

S_{1n} and S_{2n} of all the SC blocks are turned ON simultaneously for a duration $D_1 T_s$ for charging the C_T of all the SC blocks in parallel from V_{PV} . Then the input switches are turned OFF. There is a dead time t_D when all the switches S_{1n} to S_{4n} are turned OFF. After t_D , all the output switches S_{3n} and S_{4n}

are turned ON together for the interval $D_2 T_s$ to discharge C_T serially. Thus, the charge transfer capacitors C_T are switched between the input source V_{PV} and output V_O with the pulse width increasing and decreasing in a sinusoidal manner as per (1). The output ground g_o is floating with respect to the input ground g_s [see Fig. 2(b)]. This causes the series connection of all the C_T s to boost V_{PV} when the output switches are turned ON and input switches are turned OFF. The output LC filter averages the boosted SPWM pulses to yield a full-wave-rectified sine output across AB in Fig. 2(a). The unfolding circuit comprising switches U_1 to U_4 , driven as shown in Fig. 3, at a low frequency f_o unfolds alternate full-wave sine waveforms to yield a bidirectional sine output $v_o(t)$ across R_L .

As per [32], a stage of an inverter is defined as the section where high-frequency switching and power conversion is done. In the topology of Fig. 2, only the SC blocks operate at a high frequency f_s , whereas the unfolding circuit switches at a low frequency f_o . Also, the conduction losses in the unfolding stage can be minimized by choosing low R_{DS-ON} MOSFETs. Thus, the losses here are small compared to the losses in the high-frequency SC stage. Hence, it is a single-stage topology. Furthermore, since only capacitors are used in the high-frequency power conversion stage, the topology may be classified as an SC topology. An inductor is used only in the output filter to achieve a total harmonic distortion (THD) $< 5\%$.

There is a unique operating point on the array's power-voltage ($P-V$) curve called the MPP, where the power generation is maximum. The $P-V$ curve and the MPP shift, depending on the solar illumination intensity and angle, module temperature, etc. To extract the maximum power from the PV array, it is necessary

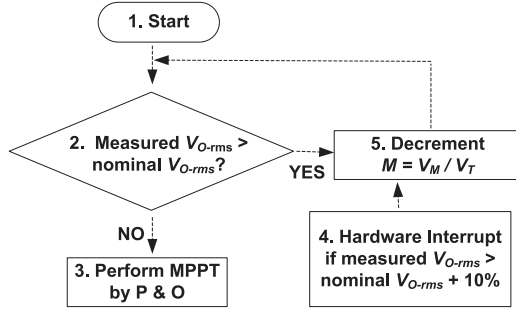


Fig. 4. Flowchart for regulating $v_O(t)$ for stand-alone operation and performing MPP tracking.

to operate the array at the MPP. The “perturb and observe” (P & O) method elaborated in [33] is employed here to track the MPP due to its simplicity. The operating point on the module’s $P-V$ curve is altered by incrementing or decrementing the modulation index $M = V_M / V_T$. When M is increased, the SPWM control pulse width increases and more power is extracted from the PV module and vice versa.

B. Output Voltage Regulation for Stand-Alone Application

As per the literature survey presented in the previous section, it is seen that most of the PV source fed inverters are grid-connected. The advantage of grid-connected systems is that since the inverter outputs are tied to the grid, the output voltage $v_O(t)$ is automatically regulated. Also, since the grid is an infinite sink, it can always absorb all the ac output power of the inverter. In a PV source fed stand-alone inverter, we have the following observations: 1) for a fixed load, $v_O(t)$ increases when the power generation from the PV source increases and vice versa; and 2) for a fixed power generation, $v_O(t)$ increases when the load decreases and vice versa. Since loads cannot tolerate a widely varying supply voltage, especially high voltages, it is mandatory to regulate the upper limit of $v_O(t)$ in stand-alone systems.

By controlling M , the MPP of the PV module is tracked and regulation of $v_O(t)$ is achieved. The rms value of the sinusoidal output (V_{O-rms}) is restricted to within +10% of the desired nominal value. In the flowchart of Fig. 4, initializations are carried out in block 1. V_{O-rms} is measured in block 2. If the measured value of $V_{O-rms} <$ the nominal rms, the standard P & O MPP tracking algorithm of block 3 tracks the MPP of the PV source. At any point of time, if the measured V_{O-rms} exceeds the nominal V_{O-rms} by 10%, a hardware interrupt (block 4) causes M to be decremented in steps (block 5). This causes the decrease of V_{O-rms} up to just below the nominal V_{O-rms} after which the P & O MPP tracking algorithm of block 3 takes over.

Two different operating modes will result due to the aforementioned algorithm. In mode 1, R_L is such that it is able to absorb all the power generated by the PV source such that V_{O-rms} will not exceed 10% of the nominal V_{O-rms} . Now, it is mandatory to track the MPP and the P & O MPP tracking algorithm of block 3 will be continuously executed. The actual value of V_{O-rms} will depend on the prevailing load on the inverter and

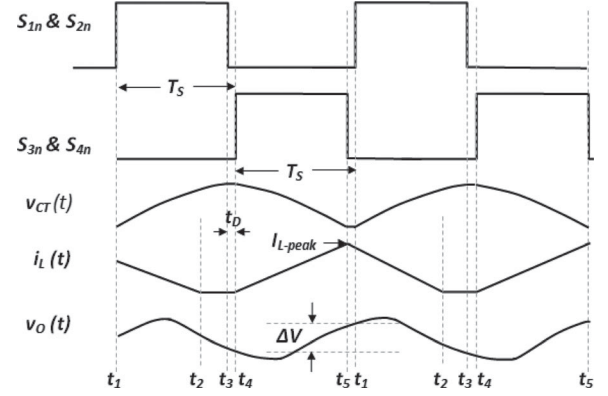


Fig. 5. Drive signals to the input switches (S_{1n} and S_{2n}) and output switches (S_{3n} and S_{4n}), charge transfer capacitor voltage $v_{CT}(t)$ across one C_T , inductor current $i_L(t)$, and output capacitor voltage $v_O(t)$.

generation from the PV module. A limit on the minimum value of V_{O-rms} has not been set. If the PV source’s MPP is not tracked in this scenario, we will be operating at a suboptimal point on the panel’s $P-V$ curve. In mode 2, the inverter may be on light load and the PV panel may be well illuminated. Now, if the MPP is tracked, the power generation will be surplus, causing a rise in V_{O-rms} . If it rises beyond $V_{O-rms} + 10\%$, the MPP is no longer tracked since the hardware interrupt causes a step-by-step decrement of M , which, in turn, leads to step-by-step reduction of V_{O-rms} . The moment the measured $V_{O-rms} <$ nominal V_{O-rms} , the P & O algorithm is executed to track the MPP. If the load continues to be light, V_{O-rms} again increases beyond $V_{O-rms} + 10\%$ and the aforementioned procedure is repeated. V_{O-rms} will continuously oscillate between the nominal value and the nominal value + 10%. Now, the module is not continuously operated at the MPP. These are shown in the experimental results in Section VI. Using instantaneous $v_O(t)$ may make the algorithm prone to spurious spikes in $v_O(t)$, whereas using V_{O-rms} will avoid this.

III. DETAILED OPERATION OF THE SINGLE-STAGE SC INVERTER TOPOLOGY

The block diagram of the SC inverter is discussed in the previous section. Here, the detailed circuit operation is examined by subdividing a complete charge–discharge cycle of time period $2T_s$ into four subintervals. The expected waveforms are given in Fig. 5. The capacitor C_{PV} [see Fig. 2(a)] connected across the PV source ensures that a steady dc voltage V_{PV} with a negligible ripple is presented to the SC inverter.

t_1 to t_2 [see Fig. 6(a)]: This is part of the interval during which the input switches S_{1n} and S_{2n} of all the SC blocks are ON and output switches S_{3n} and S_{4n} are OFF. The charge transfer capacitors C_T of all blocks are connected in parallel across the PV source and they are charged in parallel. Inductor L freewheels through diode D and supports the load R_L and charges C_O as long as $i_L(t) >$ the output current. When $i_L(t) <$ the output current, R_L is supported by both C_O and L . Finally, at $t = t_2$, $i_L(t) = 0$.

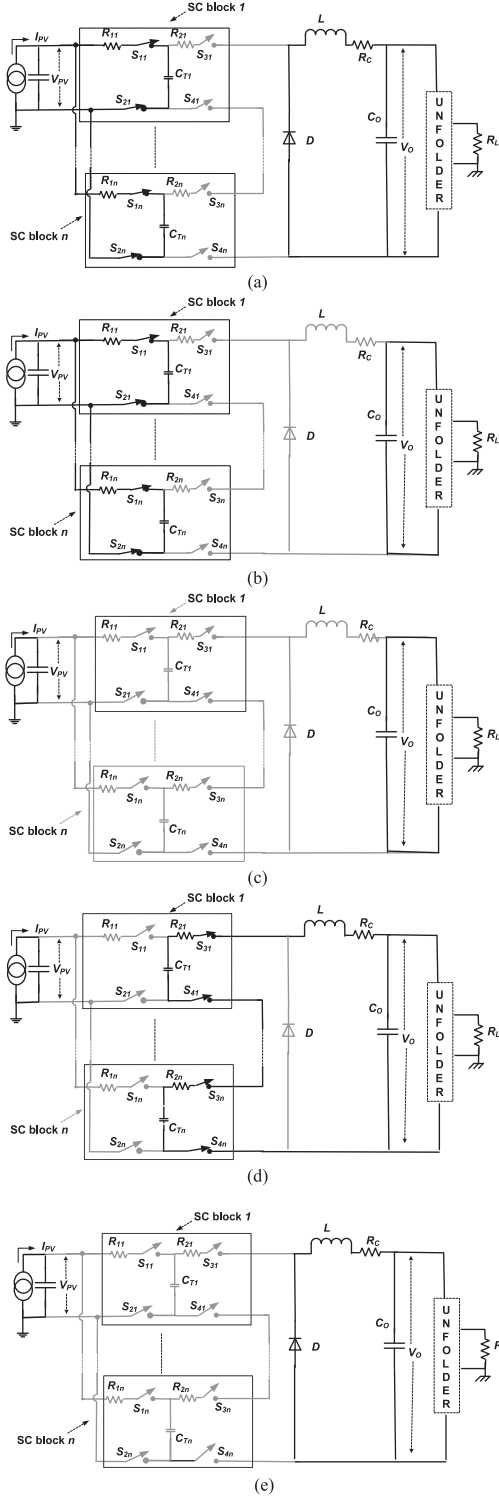


Fig. 6. Circuit configurations of the SC-based inverter during different subintervals: (a) t_1 to t_2 ; (b) t_2 to t_3 ; (c) t_3 to t_4 ; (d) t_4 to t_5 ; and (e) t_5 to t_1 : The part of the circuit shown in black color is active and the part in gray is inactive.

t_2 to t_3 [see Fig. 6(b)]: The input switches S_{1n} and S_{2n} continue to be ON, charging C_T . The output switches S_{3n} and S_{4n} continue to be OFF. Now, R_L is supported only by C_O since $i_L(t) = 0$.

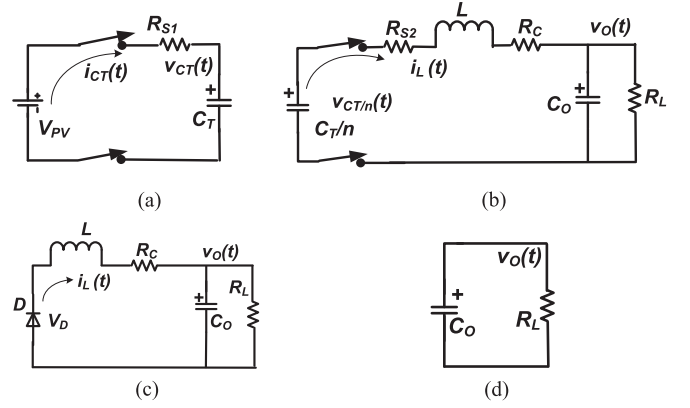


Fig. 7. Four sequential phases of the SC inverter: (a) C_T charging; (b) C_T serially discharging; (c) L freewheeling and C_O discharging; and (d) C_O discharging.

t_3 to t_4 [see Fig. 6(c)]: This is the dead time when all switches S_{1n} to S_{4n} of all the SC blocks are OFF. R_L continues to be supported only by C_O .

t_4 to t_5 [see Fig. 6(d)]: The input switches S_{1n} and S_{2n} of all the SC blocks are OFF and output switches S_{3n} and S_{4n} are ON. All C_T s are connected in series and they discharge serially into the circuit comprising L and R_C in series and C_O and R_L in shunt. $i_L(t)$ ramps up. C_O starts charging when $i_L(t) > 0$ the output current.

t_5 to t_1 [see Fig. 6(e)]: This is the dead time. All the switches S_{1n} to S_{4n} of all the SC blocks are OFF. L begins to freewheel through D .

IV. STEADY-STATE ANALYSIS AND MATHEMATICAL MODEL OF THE SINGLE-STAGE SC INVERTER TOPOLOGY

In this section, the steady-state analysis of the inverter is carried out and a mathematical model is developed. The analysis enables to understand the interdependence of various parameters and component values on the overall performance of the inverter. This is used as a quantitative tool to optimize the inverter design. The mathematical model is developed by formulating equations and solving them to determine the state variables for the four distinct sequential phases in the operation of the SC inverter. The state variables involved are charge transfer capacitor voltage $v_{CT}(t)$ during charge-up phase and $v_{CT/n}(t)$ during discharge phase (due to serial discharge), inductor current $i_L(t)$ and output capacitor voltage $v_O(t)$. Each phase and the relevant equations are given later.

Phase 1— C_T charge up [see Fig. 7(a)]: This corresponds to the time period from t_1 to t_3 in Fig. 5 during which all input switches S_{1n} and S_{2n} of all the SC blocks are ON and all the C_T s charge up in parallel from V_{PV} [see Fig. 6(a) and (b)]. Let $\tau_1 = R_{S1}C_T$, where R_{S1} is the sum of all the parasitic resistances (such as the MOSFET R_{DS-ON} , capacitor ESR, etc.) in the charging path. Let $v_{CT}(t_1)$ be the value of the voltage across each C_T at the start of the charge cycle. It is the initial value for phase 1. The state variable involved is $v_{CT}(t)$ and is given by

$$v_{CT}(t) = V_{PV} + [v_{CT}(t_1) - V_{PV}]e^{-t/\tau_1}. \quad (2)$$

At the end of the charge-up phase, $t = t_3$ and $v_{CT}(t) = v_{CT}(t_3)$.

Phase 2— C_T serial discharge [see Fig. 7(b)]: This phase corresponds to the time period from t_4 to t_5 in Fig. 5 during which output switches S_{3n} and S_{4n} of all the SC blocks are ON and all the C_T s discharge in series [see Fig. 6(d)] into the load R_L . The effective charge transfer capacitance due to the serial discharge is C_T/n . R_{S2} is the sum of the parasitic resistances in the discharging path and R_C is the series resistance of L . The state variables involved are $v_{CT/n}(t)$, $i_L(t)$, and $v_O(t)$. They are given by

$$\frac{di_L}{dt} = \frac{v_{CT/n}}{L} - \frac{i_L R_{S2}}{L} - \frac{i_L R_C}{L} - \frac{v_O}{L} \quad (3)$$

$$\frac{dv_O}{dt} = \frac{i_L}{C_O} - \frac{v_O}{R_L C_O} \quad (4)$$

$$\frac{dv_{CT/n}}{dt} = -\frac{i_L}{C_T} \quad (5)$$

Solving the aforementioned differential equations yields the expressions for the three state variables for phase 2. $i_L(t)$ is given by

$$i_L(t) = Z_1 e^{r_1 t} + e^{p_1 t} (Z_2 \cos q_1 t + Z_3 \sin q_1 t) \quad (6)$$

where the constants Z_1 to Z_3 and r_1 , p_1 , and q_1 are given by

$$Z_1 = -Z_2$$

$$= \frac{v_{CT/n}(t_4) C_{T/n} (p_1^2 + q_1^2) r_1 + \frac{[v_O(t_4) - v_{CT/n}(t_4)]}{L} r_1}{[-(r_1 - p_1) r_1 - (p_1^2 + q_1^2) + p_1 r_1]} \quad (7)$$

$$Z_3 = \frac{v_{CT/n}(t_4) C_{T/n} (p_1^2 + q_1^2)}{q_1} + \frac{Z_1 (p_1^2 + q_1^2)}{r_1 q_1}$$

$$- \frac{Z_1 p_1}{q_1} \quad (8)$$

r_1 is the real root and p_1 and q_1 are the imaginary roots of the cubic equation $x^3 + K_2 x^2 + K_1 x + K_0 = 0$ where

$$K_2 = \left(\frac{1}{C_O R_L} + \frac{R_{S2}}{L} + \frac{R_C}{L} \right) \quad (9)$$

$$K_1 = \left(\frac{R_{S2}}{C_O R_L L} + \frac{R_C}{C_O R_L L} + \frac{1}{L(C_T/n)} + \frac{1}{L C_O} \right) \quad (10)$$

$$K_0 = \frac{1}{C_O R_L L(C_T/n)} \quad (11)$$

$v_O(t_4)$ is the final value of $v_O(t)$ at the end of the C_O discharge phase. Due to the discontinuous operation of L , $i_L(t_4) = 0$. $v_{CT/n}(t_4)$ is the voltage across the series-connected charge transfer capacitors at $t = t_4$, which is derived from the final value of $v_{CT}(t)$ at the end of phase 1. These are the initial values for phase 2.

Equations (12) and (13) given in the Appendix are the expressions for the other state variables $v_{CT/n}(t)$ and $v_O(t)$.

Phase 3— L freewheeling and C_O discharging [see Fig. 7(c)]: This phase corresponds to the time period from t_5 to t_2 in Fig. 5. It overlaps with part of phase 1 [see Fig. 6(a)]. V_D

denotes the drop across the diode D . The state variables involved are $i_L(t)$ and $v_O(t)$. They are given by

$$\frac{di_L}{dt} = -\frac{i_L R_C}{L} - \frac{v_O}{L} - \frac{V_D}{L} \quad (14)$$

$$\frac{dv_O}{dt} = \frac{i_L}{C_O} - \frac{v_O}{R_L C_O} \quad (15)$$

Solving (14) and (15) yields the expressions for $i_L(t)$ and $v_O(t)$

$$i_L(t) = e^{p_2 t} (Z_4 \cos q_2 t + Z_5 \sin q_2 t) - \frac{V_D}{L C_O R_L} \frac{1}{m_1 m_2} \quad (16)$$

where the constants Z_4 and Z_5 and m_1 and m_2 are given by

$$Z_4 = i_L(t_5) + \frac{V_D}{L C_O R_L} \frac{1}{m_1 m_2} \quad (17)$$

$$Z_5 = -\frac{v_O(t_5) + L Z_4 p_2 + R_C Z_4 + \frac{R_C V_D}{L C_O R_L} \frac{1}{m_1 m_2} + V_D}{L q_2} \quad (18)$$

$m_1 = p_2 + i q_2$ and $m_2 = p_2 - i q_2$ where

$$p_2 = \frac{-\left(\frac{R_C}{L} + \frac{1}{R_L C_O}\right)}{2} \quad (19)$$

$$q_2 = \frac{\sqrt{\left(\frac{2}{\sqrt{L C_O}}\right)^2 - \left(\frac{R_C}{L} - \frac{1}{R_L C_O}\right)^2}}{2} \quad (20)$$

The state variable $v_O(t)$ is given by (21) in the Appendix.

In (17) and (18), $i_L(t_5)$ and $v_O(t_5)$ are the final values of $i_L(t)$ and $v_O(t)$ at the end of phase 2, i.e., at $t = t_5$. These are the initial values for phase 3.

Phase 4— C_O discharging [see Fig. 7(d)]: This phase corresponds to the time period from t_2 to t_4 in Figs. 5 and 6(b) and (c) when $i_L(t) = 0$. Now, R_L is supported only by C_O . Let $\tau_2 = R_L C_O$. $v_O(t_2)$ is the final value of $v_O(t)$ in phase 3. It is the initial value of $v_O(t)$ in phase 4. The state variable involved in this phase is $v_O(t)$ and is given by

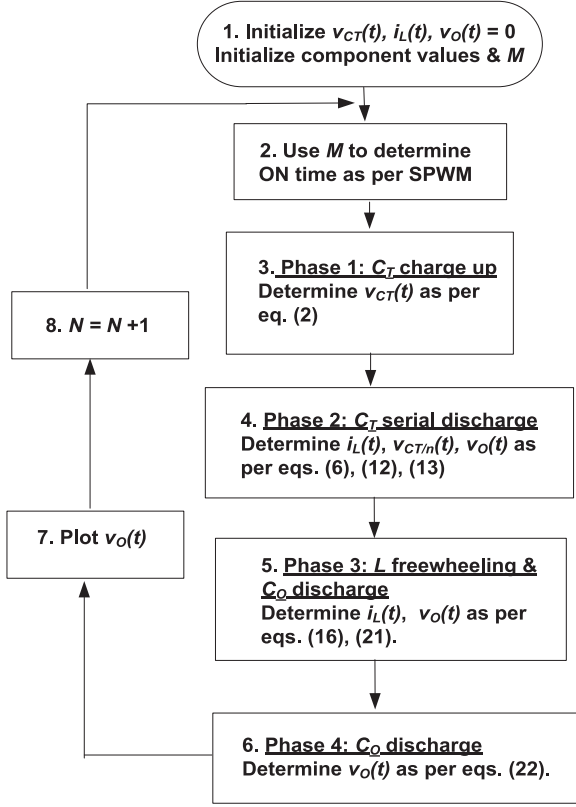
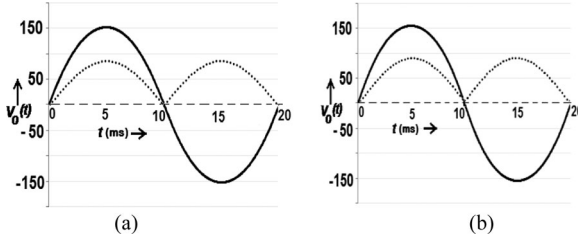
$$v_O(t) = v_O(t_2) e^{-t/\tau_2} \quad (22)$$

V. APPLICATIONS OF THE MATHEMATICAL MODEL

The applications of the steady-state analysis and mathematical model based on (1)–(22) developed in the previous section are discussed in detail in this section. For a given operating condition, the model enables the determination of the state variables viz. $v_O(t)$, $i_L(t)$, and $v_{CT}(t)$ at any given time. This is used to analyze the inverter performance and optimize the component choice.

A. Validating the Mathematical Model

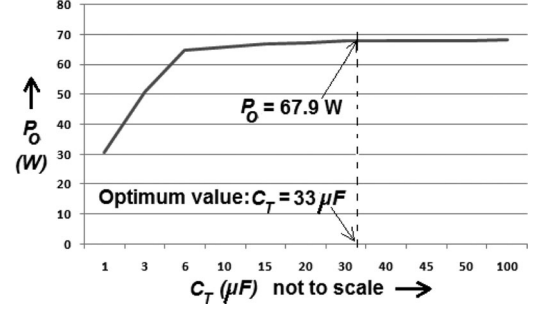
At the outset, the validity of the mathematical model of the SC inverter is established by examining the inverter output $v_O(t)$ which must be a sine waveform. The equations of the state variables that describe each phase of operation of the inverter are solved sequentially to determine the value of the state variables

Fig. 8. Flowchart for plotting $v_O(t)$ using the mathematical analysis.Fig. 9. (a) and (b) Output $v_O(t)$ of the flowchart of Fig. 8. The full-wave rectified sine reference is shown in dotted trace. (a) $P_O = 66$ W, $V_{PV} = 60$ V; theoretical THD = 4.03%. (b) $P_O = 33$ W, $V_{PV} = 55$ V, theoretical THD = 5.01%. In both cases, $v_O(t) \approx 110$ Vrms at 50 Hz.

at the end of the respective phase. Initially, zero initial values are assumed for the state variables. Later, the final values of the state variables involved in each phase are used as the initial values in the following phase. This process is outlined in the flowchart of Fig. 8. When the loop is executed f_s/f_o times by incrementing N , a complete cycle of the steady-state output $v_O(t)$ is generated by plotting $v_O(t)$ in every alternate iteration of the loop since its periodicity is $f_s/2$.

$v_O(t)$ plotted in Fig. 9(a) and (b) are the outputs of the flowchart of Fig. 8 for different PV module illumination conditions. M and C_O are adjusted to get the desired $v_O(t)$. All other parameters and component values are the same.

The THD of $v_O(t)$ gives the measure of its quality. The flowchart of Fig. 8 generates a vector of $f_s/2f_o$ points that represents one cycle of $v_O(t)$. The theoretical THD of $v_O(t)$ is determined with MATLAB. An *m-file* is used to

Fig. 10. Optimization of C_T for a desired input and output specification.

determine the discrete Fourier transform of the vector representing $v_O(t)$. The location of the fundamental is ascertained as it has the maximum amplitude. Then the location of the harmonics is determined. Finally, the THD is computed from the square of the amplitude of the fundamental and its harmonics. The THD of $v_O(t)$ of Fig. 9(a) is 4.03%, while that of Fig. 9(b) is 5.01%.

The following conclusions may be derived from these observations: 1) SPWM generates a boosted sinusoidal output $v_O(t)$ when applied to the SC topology of Fig. 2; and 2) M and C_O may be adjusted to generate a pure sine output for different input and load conditions.

Hence, the mathematical model and analysis is validated and may be used for further studies.

B. Analysis and Optimization of the SC Inverter

The possibility to determine any of the state variables at any desired time under a given operating condition with the flowchart of Fig. 8 forms the basis of the methods presented in this section for analysis and optimization. Due to SPWM, the state variables do not attain a fixed steady-state value as in dc-dc converters. Hence, a graphical method is presented to optimize the component values.

The average output power P_O is given by

$$P_O = \frac{V_{O-rms}^2}{R_L} = \frac{V_{O-peak}^2}{2R_L} = \frac{\left(v_O(t) \Big|_{N=\frac{f_s}{4f_o}}\right)^2}{2R_L} \quad (23)$$

where the value of $v_O(t)$ evaluated at $N = f_s/4f_o$ corresponds to the peak output value V_{O-peak} .

1) Optimizing C_T : C_T used in each SC block (see Fig. 6) is responsible for transferring power from the PV source to the load. It has to handle a large current ripple. Hence, a low ESR ceramic or metalized polyester capacitor is used. For a cost-effective design, the capacitors have to be optimized. To optimize C_T for a given operating condition, P_O is determined for different values of C_T under the given operating condition. The variation of P_O with C_T is studied, as shown in Fig. 10. Initially, P_O increases steadily when C_T is increased. Beyond a certain value, P_O almost stabilizes even if C_T continues to increase due to the fact that the increase in C_T is now offset by the decrease in ΔV_{CT} limiting the charge transfer $Q_{CT} = C_T \cdot \Delta V_{CT}$ in each cycle. This shows that it is possible to choose an optimum value of C_T for a desired P_O .

2) Optimizing MOSFETs: MOSFET switches are usually used in SC power conditioners. MOSFET optimization implies choosing MOSFETs with lowest V_{DS} and I_{DS} ratings and highest R_{DS-ON} rating to meet the required design since MOSFETs with higher V_{DS} and I_{DS} and lower R_{DS-ON} are more expensive due to larger die size. MOSFET R_{DS-ON} optimization in this context refers to choosing the MOSFETs with the highest R_{DS-ON} that meet the initial design assumptions. If MOSFETs with lower R_{DS-ON} are used in the charging circuit [see Fig. 7(a)], the efficiency does not improve since charging circuit resistances do not play a part in the capacitor charging efficiency [4]. The optimum R_{DS-ON} MOSFET in charging circuit will enable to extract the MPP power at maximum M . Using MOSFETs with lower than optimum R_{DS-ON} will result in operating at the MPP even at lower than maximum M . However, using lower R_{DS-ON} MOSFETs in the discharging circuit will marginally increase the efficiency and the inverter will be able to deliver more output power than the initial design assumptions when operating at the maximum value of M . The input MOSFETs (S_{1n} and S_{2n} of Fig. 6) are chosen so that $I_{DS} > i_{CTmax}(t)$ where [referring to Figs. 5 and 7(a) and (2)]

$$I_{DS} > i_{CTmax}(t) = \frac{V_{PV} - v_{CT}(t_1)|_{N=f_s/4f_o}}{R_{S1}}. \quad (24)$$

The second term in the numerator corresponds to the value of $v_{CT}(t)$ at $t = t_1$ evaluated at $N = f_s/4f_o$. This is the lowest value of $v_{CT}(t)$ causing the highest value of $i_{CT}(t)$. Since MPP is tracked, the operating point on the array is at V_{MPP} . The maximum voltage that the input MOSFETs (S_1 and S_2 of Figs. 6 and 13) must block depends on V_{MPP} and the number of SC blocks n . During the discharge phase, n C_T s that are charged to V_{MPP} are connected in series. Now, the maximum voltage that each of the output MOSFETs (S_3 and S_4 of Figs. 6 and 13) have to block is nV_{MPP} . For output MOSFETs, $I_{DS} > 4I_{Opeak}$ since L operates in discontinuous mode. R_{S1} represents the parasitic resistances in the charging path, including the sum of MOSFET ON resistances in the charging circuit, and R_{S2} represents the parasitic resistances in the discharging path including the sum of MOSFET ON resistances in the discharging circuit. For a given operating condition, P_O is plotted for different values of R_{S1} and R_{S2} in Fig. 11. P_O decreases with increase in R_{S1} and R_{S2} since Q_{CT} decreases with increase of resistance in the charge path. From this figure, it is possible to determine optimum values of R_{S1} and R_{S2} that meet the required operating specifications.

3) Optimizing C_O : C_O affects the average output ripple ΔV . Referring to Fig. 5, R_L is supported by L and C_O during the time period t_5 to t_4 . When $v_O(t) = V_{O-peak}$, the duty ratio is maximum, and if we neglect the dead time t_D , the time duration between t_5 and t_4 is T_S . In Step 2 (Design of L) of the design procedure given later, it is given that L operates in discontinuous mode such that $i_L(t) = 0$ in $2/3T_S$. Now, R_L is supported fully by C_O for about $0.5T_S$. Thus, C_O is given by

$$C_O = \frac{-0.5T_S}{R_L \times \ln\left(\frac{V_{O-peak} - \Delta V}{V_{O-peak}}\right)}. \quad (25)$$

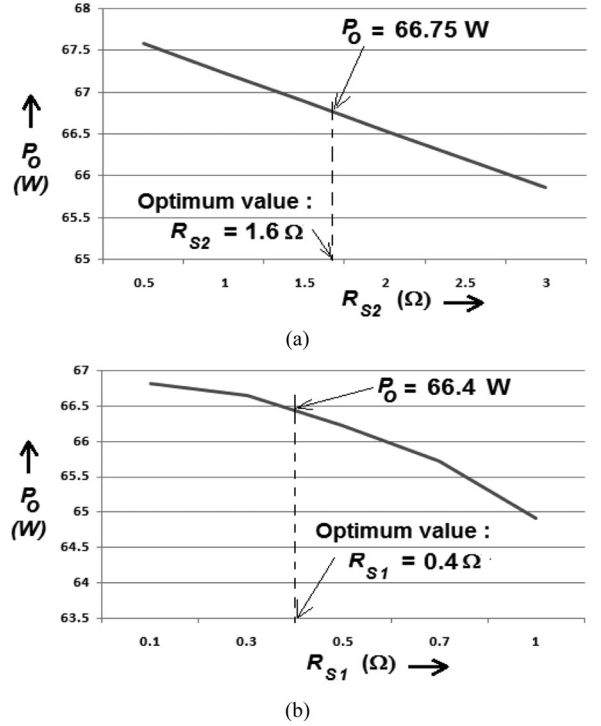


Fig. 11. Optimization of (a) R_{S2} and (b) R_{S1} for a desired input and output specification.

Crossover distortion $V_{crossover}$ refers to $v_O(t)$ evaluated at $N = 1$. It is given by

$$V_{crossover} = v_O(t)|_{N=1}. \quad (26)$$

Ideally, $V_{crossover} = 0$. Nonzero $V_{crossover}$ deteriorates the THD. A higher C_O results in a lower ΔV but larger $V_{crossover}$ and vice versa. From (22), it is seen that R_L has a strong influence on $v_O(t)$. Hence, it is essential to change C_O dynamically, depending on R_L to keep $V_{crossover}$ to a minimum and, hence, the THD within desired limits.

VI. EXPERIMENTAL RESULTS

This section presents the following: 1) a stepwise design procedure for the choice of optimum components for the SC inverter based on the graphical analysis and optimization methods discussed in the previous section; and 2) experimental waveforms of the hardware prototype and correlation with the theoretical aspects.

A. Stepwise Design Procedure for the SC Inverter

Input and Output Specifications

The aim is to design a single-stage SC inverter of Fig. 6 that operates on a PV module with $35 \text{ W} \leq P_{MPP} \leq 70 \text{ W}$ and $55 \text{ V} \leq V_{MPP} \leq 60 \text{ V}$ with variation of the intensity of solar illumination. The desired ac output under nominal operating conditions is 50 Hz sine with $V_{0-rms} = 110 \text{ V} \pm 10\%$ and THD $\leq 5\%$.

Step 1—Selecting C_{PV} : A constant voltage must be presented to the input of the SC inverter. A capacitor C_{PV} (see Fig. 2) is connected across the PV module's output for this purpose

where [31]

$$C_{PV} = \frac{P_{PV}}{4\pi f_O V_{PV} \Delta V_{PV}}. \quad (27)$$

Here, P_{PV} is the maximum power that the PV array can deliver and ΔV_{PV} is the maximum allowed ripple on the PV voltage V_{PV} . Allowing $\Delta V_{PV} \approx 2\%$ of V_{PV} , $C_{PV} \approx 1800 \mu\text{F}$ is chosen.

Step 2—Design of L : Let $f_S = 35 \text{ kHz}$. L is designed to always operate in discontinuous conduction mode to minimize its size. Let $I_{L-\text{peak}}$ be the peak value of $i_L(t)$. It is assumed that $I_{L-\text{peak}} = 4I_{O-\text{peak}}$. Take efficiency $\eta \approx 95\%$. When $P_{MPP} = 70 \text{ W}$, $I_{O-\text{peak}} = 0.87 \text{ A}$. Referring to Fig. 5, $i_L(t)$ begins to ramp down from $I_{L-\text{peak}}$ to zero after the output MOSFETs turn OFF at t_5 . Assume that this ramp down of $i_L(t)$ is accomplished in $0.65T_S$ (i.e., $2/3T_S$). Now, $L = (V_{O-\text{peak}} \cdot dt/di) \approx 850 \mu\text{H}$, where $dt = 0.65T_S$ and $di = 4I_{O-\text{peak}}$. A toroidal core is used to realize the inductor. Coil resistance $R_C \approx 0.2 \Omega$.

Step 3—Determine n (The Number of SC Blocks): n SC blocks [see Fig. 2(b)] are connected, as in Fig. 6, to boost the input voltage. Minimum value of n has to be determined so that the desired $V_{O-\text{rms}} = 110 \text{ V}$ may be achieved for the peak output load of 66 W corresponding to $R_L = 180 \Omega$. If $\Delta V \approx 7\%$ of $V_{O-\text{peak}}$ is allowed, then using (25), C_O is approximately $0.75 \mu\text{F}$. Make an initial assumption of $C_T = 100 \mu\text{F}$ and $R_{S1} = R_{S2} = 0.1 \Omega$. From Step 2, $L = 850 \mu\text{H}$ and $R_C = 0.2 \Omega$. The algorithm of Fig. 8 is executed to determine $V_{O-\text{rms}}$ for different values of n with the maximum value of M , i.e., $M = 0.95$ and $V_{PV} = 60 \text{ V}$. For $n = 1$, $V_{O-\text{rms}} = 27.58 \text{ V}$. For $n = 2$, $V_{O-\text{rms}} = 56 \text{ V}$, and for $n = 3$, $V_{O-\text{rms}} = 84 \text{ V}$. When $n = 4$, $V_{O-\text{rms}} = 111.7 \text{ V}$. This is above our requirement of $V_{O-\text{rms}} = 110 \text{ V}$. Thus, we choose $n = 4$ to meet the required specifications.

Step 4—Selecting Optimum C_T : In Fig. 10, P_O is plotted for different values of C_T . The operating conditions assumed are $V_{PV} = 60 \text{ V}$, $R_{S1} = R_{S2} = 0.1 \Omega$, $C_O = 0.75 \mu\text{F}$, and $M = 0.95$. From Step 2, $L = 850 \mu\text{H}$ and $R_C = 0.2 \Omega$. From Step 3, $n = 4$. Required $V_{O-\text{rms}} \approx 110 \text{ V}$ and $P_O \approx 66 \text{ W}$. C_T is varied from 1 to $100 \mu\text{F}$. From Fig. 10, $C_T = 33 \mu\text{F}$ is the optimum choice. With this value we can meet the requirement of $P_O \approx 66 \text{ W}$ at $V_{O-\text{rms}} = 110 \text{ V}$. A metallized polyester capacitor (Euro Farad PM90R1S) is used due to its very low ESR ($\approx 4 \text{ m}\Omega$) and high ripple current rating.

Step 5—Selecting Optimum MOSFETs: $R_{S2} = (\sum R_{DS-\text{ON}}$ of output side MOSFETs + parasitic resistances in discharge path). $R_{S1} = (\sum R_{DS-\text{ON}}$ of input-side MOSFETs + parasitic resistances in the charging path). The MOSFET $R_{DS-\text{ON}}$ is the major factor influencing R_{S1} and R_{S2} . As in Step 4, a graphical method is adopted to select the optimum MOSFET $R_{DS-\text{ON}}$.

First, it is assumed that $R_{S1} = 0.1 \Omega$. P_O is plotted in Fig. 11(a) for the same operating conditions and output specifications as in Step 4 except that now $C_T = 33 \mu\text{F}$. R_{S2} is varied such that $0.5 \Omega \leq R_{S2} \leq 3 \Omega$. Fig. 11(a) shows that even when R_{S2} varies from 0.2 to 3Ω , P_O changes by only about 2 W . For $P_O \approx 66 \text{ W}$, R_{S2} may be fixed at 1.6Ω . IRFM360 is chosen as the output MOSFET. It has an $R_{DS-\text{ON}} = 0.2 \Omega$.

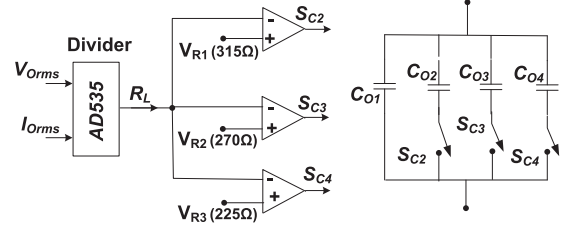


Fig. 12. Determination of C_O depending on R_L .

During the discharge phase, the eight output MOSFETs S_{31}, S_{41} , etc. (see Fig. 6) are in series. Hence, total $R_{DS-\text{ON}} = 1.6 \Omega$. Required $V_{DS} = nV_{MPP} = 4 \times 60 \text{ V} = 240 \text{ V}$, where n is the number of SC blocks. V_{DS} of IRFM360 that is selected is 400 V . Also, $I_{DS} = 23 \text{ A}$, which is well above the required value of $4I_{O-\text{peak}} = 3.5 \text{ A}$. Capacitor ESR is negligible.

Next, R_{S2} is fixed at 1.6Ω and R_{S1} is varied such that $0.1 \Omega \leq R_{S1} \leq 1 \Omega$. P_O is plotted against R_{S1} in Fig. 11(b). For $P_O \approx 66 \text{ W}$, R_{S1} may be fixed at 0.4Ω . IRF6215 ($R_{DS-\text{ON}} = 0.3 \Omega$) is chosen as the high-side input MOSFET (S_{1n}). The simple drive circuit for a p-channel device in this location is the reason for choosing it. IRFB52N15D ($R_{DS-\text{ON}} = 0.03 \Omega$) is chosen as the low-side input MOSFET (S_{2n}). In this implementation, $n = 4$. Analysis of Fig. 13 shows that a maximum reverse voltage of $2V_{MPP} = 2 \times 60 \text{ V}$ develops across some of the input MOSFETs when C_T s are connected in series during the discharge. Hence, MOSFETs with $V_{DS} > 2V_{MPP}$ are chosen as the input MOSFETs (S_1, S_2 , etc.). The input MOSFETs that are selected have a $V_{DS} = 150 \text{ V}$. Using (24), $i_{C_T \text{ max}}(t) = 3.12 \text{ A}$, which is well below the I_{DS} of the MOSFETs considered.

Step 6—Choosing C_O : Let $\Delta V = 10 \text{ V}$ ($\approx 7\%$ of $V_{O-\text{peak}}$). Similar ripple is observed in [12] and [31]. At maximum load, $R_L = 180 \Omega$ ($P_O = 67 \text{ W}$). Using (25), $C_O = 0.75 \mu\text{F}$. Since C_O affects $V_{\text{crossover}}$ and, hence, the THD also, it is mandatory that C_O be changed dynamically depending on R_L . The PV module's P_{MPP} varies such that $35 \text{ W} \leq P_{MPP} \leq 70 \text{ W}$. Assuming $\eta \approx 95\%$, $360 \Omega \leq R_L \leq 180 \Omega$. This range is subdivided into four smaller ranges. Table I gives the values of C_O for these ranges of R_L that are chosen to keep the THD $\approx 5\%$.

The output capacitor C_O is determined by a network similar to that in [34] such that $C_O = C_{O1} + C_{O2} + C_{O3} + C_{O4}$ where $C_{O1} = 0.37 \mu\text{F}$ and $C_{O2} = C_{O3} = C_{O4} = 0.13 \mu\text{F}$. As shown in Fig. 12, C_{O1} is permanently hardwired to the circuit whereas the other three capacitors are included or excluded with low $R_{DS-\text{ON}}$ MOSFETs to adjust the overall value of C_O . Ceramic capacitors are used due to their low ESR (typically a few milliohms). An analog divider (AD 535) determines R_L by dividing $V_{O\text{rms}}$ by $I_{O\text{rms}}$. R_L , which is represented by a voltage, is compared by three different comparators to the different reference levels set for each of them. Reference V_{R1} is a voltage that corresponds to 315Ω , V_{R2} corresponds to 270Ω and V_{R3} corresponds to 225Ω . When $180 \Omega \leq R_L < 225 \Omega$, S_{C2} to S_{C4} are ON and $C_O = 0.75 \mu\text{F}$. When $225 \Omega \leq R_L < 270 \Omega$, S_{C4} is OFF and S_{C2} and S_{C3} are ON. Now, $C_O = 0.62 \mu\text{F}$. When

TABLE I
SUMMARY OF OPERATING SPECIFICATIONS AND COMPONENTS SELECTION

Input specifications: $35 \text{ W} \leq P_{MPP} \leq 70 \text{ W}$, $55 \text{ V} \leq V_{MPP} \leq 60 \text{ V}$ Output specifications: 50 Hz sine , $V_{0-rms} = 110 \text{ V} \pm 10\%$, $\text{THD} \leq 5\%$.								
C_{PV}	n	Input MOSFETs	Output MOSFETs	C_T	L	R_C	C_O	Worst case theoretical THD
1800 μF	4	$R_{S1} = 0.4 \Omega$ IRF6215 IRFB52N15D	$R_{S2} = 1.6 \Omega$ IRFM360	33 μF	850 μH	0.2 Ω	0.75 μF for Range 1* 0.62 μF for Range 2* 0.5 μF for Range 3* 0.37 μF for Range 4*	4.7% 5.01% 5.07% 5.15%

*Range 1: $180 \Omega \leq R_L < 225 \Omega$; Range 2: $225 \Omega \leq R_L < 270 \Omega$; Range 3: $270 \Omega \leq R_L < 315 \Omega$; Range 4: $315 \Omega \leq R_L < 360 \Omega$.

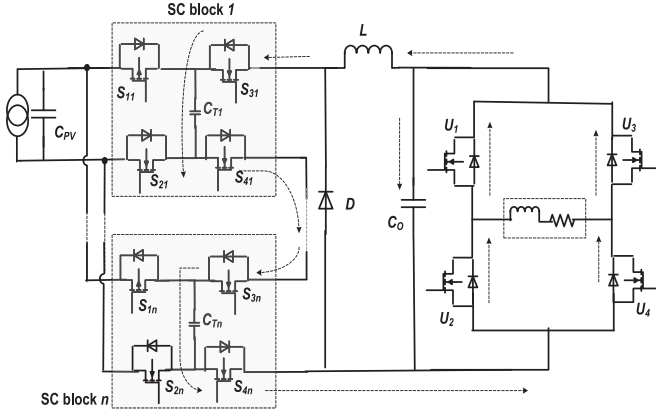


Fig. 13. Actual implantation of the SC blocks and unfolding circuit with MOSFETs. The dotted arrows show the flow of reactive current.

$270 \Omega \leq R_L < 315 \Omega$, S_{C4} and S_{C3} are OFF and $C_O = 0.5 \mu\text{F}$. When $315 \Omega \leq R_L < 360 \Omega$, S_{C4} , S_{C3} , and S_{C2} are OFF and $C_O = 0.37 \mu\text{F}$.

Table I summarizes the specifications and components finalized as per the steps formulated earlier. Fig. 13 shows the actual implementation of the SC blocks and the unfolding circuit with MOSFETs. In block 1, S_{11} and S_{21} are reversed when compared to the other blocks.

B. Experimental Waveforms of the Hardware Model

The experimental setup consists of a tunable solar array simulator to simulate the PV module operating under different conditions of solar illumination. The number of SC blocks n will have to be increased if the voltage from an actual PV module is lower than that of the simulator used here. A supervisory PC executes the algorithm of Fig. 4 implemented in C language. I_{PV} and V_{PV} are monitored and used by the P & O algorithm. $v_O(t)$ and $i_O(t)$ are also monitored to compute the value of the existing load for dynamically selecting C_O as per Table I and for limiting the upper value of $v_O(t)$ to within 10% of V_{0-rms} . Hall effect sensors are used to sense I_{PV} and $i_O(t)$. The hardware interrupt of the PC is used to execute block 4 of the algorithm to regulate $v_O(t)$. The PC generates a signal directly proportional to V_M [see (1)] that controls the amplitude of the full-wave-rectified sine reference generated by a signal generator with an IEEE interface. This reference is compared with a triangular carrier at 35 kHz to generate the drive pulses. A gating circuit channelizes alternate drive signals to the input

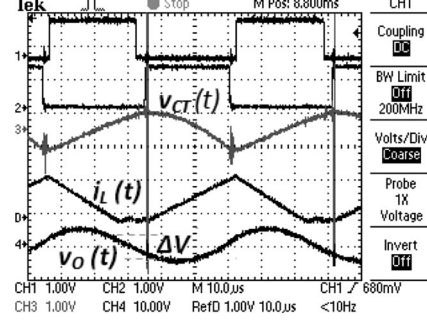


Fig. 14. Experimental waveforms: Gate drive to the input and output MOSFETs (channels 1 and 2), charge transfer capacitor voltage across one C_T $v_{CT}(t)$, inductor current $i_L(t)$ (3 A/div) and output capacitor voltage $v_O(t)$ observed in 10 $\mu\text{s}/\text{div}$ time scale. Only the ac components of $v_{CT}(t)$ and $v_O(t)$ are shown.

side MOSFETs and the output side MOSFETs. By detecting the zero crossings of the sine reference, the switches of the unfolding circuit are operated to unfold the alternate halves of the sine output.

Fig. 14 shows waveforms of the drive to the input and output MOSFETs and the state variables $v_{CT}(t)$, $i_L(t)$, and $v_O(t)$ acquired from the hardware model at a peak duty ratio. As desired, L operates in discontinuous current mode. $i_L(t) \rightarrow 0$ in about 20 μs , which is approximately $0.65 T_S$ as per step 2 of the design procedure. For $C_O = 0.75 \mu\text{F}$, ΔV given by (25) evaluates to 10 V. From Fig. 14, the measured $\Delta V \approx 10 \text{ V}$.

In Fig. 15, the 100-Hz full-wave-rectified sine reference is superimposed on the 35 kHz triangular carrier and plotted along with $v_O(t)$. A distortion analyzer (TEK AA501) is used to measure the THD of $v_O(t)$. The solar array simulator is operated to simulate different illumination conditions. R_L is manually adjusted to represent loads corresponding to ranges 1, 3, and 4 of Table I. The control circuit chooses the appropriate M and C_O in each case.

The voltage and current ripple (ΔV_{PV} and ΔI_{PV}) on the PV source at full illumination due to the switching in the SC inverter are shown in Fig. 16. As per (27), ΔV_{PV} is limited to $<2\%$ of V_{PV} due to $C_{PV} = 1800 \mu\text{F}$. The deviation from P_{MPP} due to ΔV_{PV} and ΔI_{PV} is $<1\%$. The peak MOSFET current is about 3 A, as predicted by (24).

$v_O(t)$ with inductive load is shown in Fig. 17. The path of the reactive current is shown in Fig. 13. The body diodes of the MOSFETs allow the reactive current to find a path through the

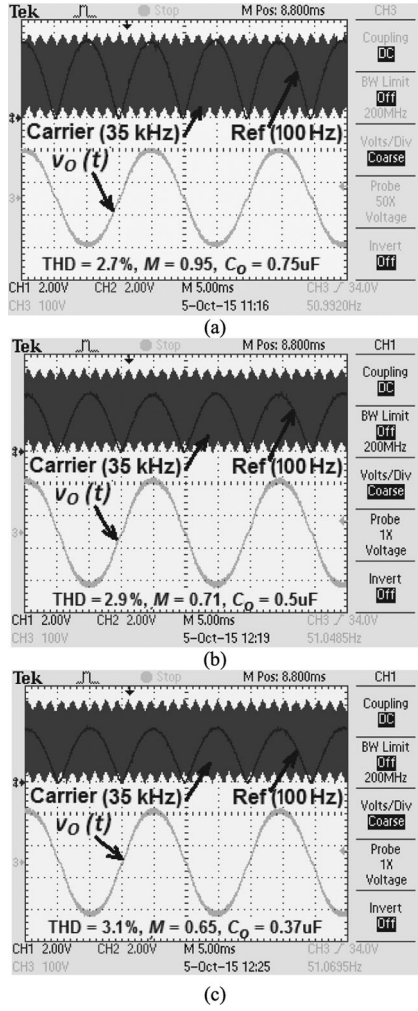


Fig. 15. Experimental waveforms: 100 Hz full-wave-rectified sine reference superimposed on 35 kHz triangular carrier and inverter output $v_O(t)$ observed in 5 ms/div time scale for different solar illumination conditions (a) $V_{PV} = 60$ V, $I_{PV} = 1.14$ A, $P_O = 65.4$ W (b) $V_{PV} = 58$ V, $I_{PV} = 0.82$ A, $P_O = 44.8$ W (c) $V_{PV} = 55$ V, $I_{PV} = 0.66$ A, $P_O = 33.6$ W. In all three cases $V_{O-rms} = 110$ V \pm 10%.

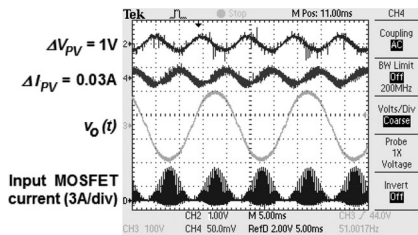


Fig. 16. Experimental waveforms: Voltage ripple (ΔV_{PV}) and current ripple on PV module (ΔI_{PV}) for full illumination. $v_O(t)$ and current through input MOSFET of one block of the SC inverter are also shown.

series-connected C_T s and C_O . As the power factor decreases, the distortion in $v_O(t)$ increases, as shown in Fig. 17(a) and (b).

The transient and steady-state performance of the MPP tracking inverter under different conditions is shown in Fig. 18. In Fig. 18(a), turn-ON behavior of the inverter at full load

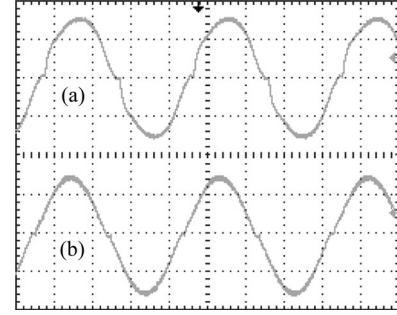


Fig. 17. Experimental waveforms: $v_O(t)$ with an inductive load. (a) $R = 146$ Ω , $L = 434$ mH, $\cos \phi = 0.73$ (b) $R = 192$ Ω , $L = 177$ mH, $\cos \phi = 0.96$.

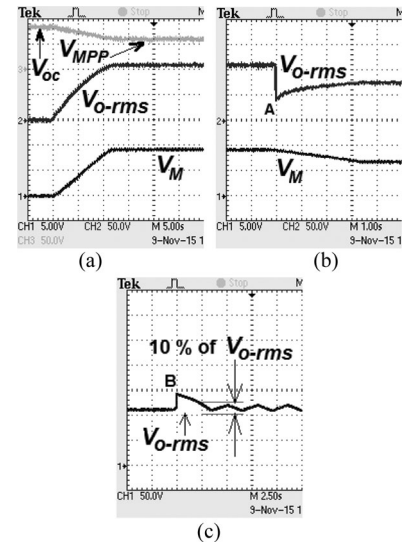


Fig. 18. Experimental waveforms: Transient and steady-state behavior of the MPP tracking SC inverter. (a) Turn ON behavior: PV source illuminated with full intensity with inverter on full load. (b) Transient behavior: Full intensity illumination and full load to low intensity illumination and full load. (c) Stand-alone operating capability: Full intensity illumination and low load - V_{O-rms} maintained within +10% of nominal value.

with the PV module illuminated at full intensity is examined. Now, the P & O algorithm (block 3 of Fig. 4) is executed. V_M is incremented/decremented by 0.5% once in 60 ms to track the MPP. Hence, it takes about 12 s to increment V_M from minimum to maximum value and consequently $M = V_M/V_T$ from 0 to 0.95. At full intensity of illumination and inverter at full load, V_M has to be set very close to the maximum value to track the MPP.

In Fig. 18(b), the inverter is initially operating at full load with a fully illuminated PV module. Now, $V_{O-rms} \approx 110$ V and $P_{MPP} \approx 69$ W. The illumination intensity is suddenly reduced at point A such that the I - V curve is altered and the new $P_{MPP} \approx 37$ W. Initially, V_{O-rms} falls since the value of V_M at point A causes off-optimal operation on the new I - V curve. When the P & O algorithm readjusts V_M for operation at the new P_{MPP} , more power is delivered to the load and V_{O-rms} increases. However, the new value of $V_{O-rms} \approx 75$ V as compared to the nominal value of 110 V. The mea-

TABLE II
SC-BASED DC-AC INVERTERS AND PV SOURCE FED IMPLEMENTATIONS

Reference no.	Powered from	Function	Remarks
[11]–[14], [16]–[20]	Voltage source	DC to ac	Boost type
[15]	Voltage source	DC to ac	Buck type
[23], [24]	PV source	MPPT + dc to dc	Unregulated output
[25]	PV source	Distributed MPPT by dc–dc conversion	Voltage equalization method (buck-type dc–dc)
[26]	Voltage source	Distributed MPPT by dc–dc conversion	Current equalization method (buck type dc–dc)
[27]	PV source	Distributed MPPT by dc–dc conversion	Buck-type dc–dc
[28]	PV source	MPPT + dc to ac	Double-stage, boost-type, grid-connected implementation
[29]	PV source	MPPT + dc to ac	Single-stage, buck-type, grid-connected implementation
[30]	PV source	MPPT + dc to ac	Double-stage, boost-type, grid-connected implementation
Proposed configuration	PV source	MPPT + dc to ac	Single-stage, boost-type, stand-alone implementation

sured MPP tracking efficiency (ratio of input power of the SC inverter to the actual MPP power of the PV module) in the earlier cases is $>97\%$.

The test condition of Fig. 18(c) shows the stand-alone operating capability of the proposed SC inverter when illumination intensity is high but load is low. At point B, R_L is suddenly reduced from about $180\ \Omega$ (full load) to about $360\ \Omega$ (minimum load). This causes V_{O-rms} to initially shoot up to 135 V due to surplus power from the PV module. Now, the hardware interrupt causes block 5 of the algorithm of Fig. 4 to be executed. Consequently V_T is decremented by 0.5% once every 60 ms by block 5 of the algorithm and V_{O-rms} gradually decreases to the nominal value of 110 V.

Once $V_{O-rms} = 110$ V, the P & O algorithm (block 3 of Fig. 4) is executed resulting in gradual increase of V_{O-rms} as the MPP is approached. When $V_{O-rms} > \text{nominal } V_{O-rms} + 10\%$, the hardware interrupt leads to execution of block 5. Thus, V_{O-rms} oscillates in a band between V_{O-rms} and $V_{O-rms} + 10\%$, as shown in Fig. 18(c). But for this scheme, V_{O-rms} will remain well above the nominal value for low loads preventing stand-alone operation. Fig. 18(a) and (b) pertains to operation in mode 1 of Section II B, while Fig. 18(c) is an example of operation in mode 2.

The inversion efficiency of the proposed single-stage SC-based scheme is plotted for different output powers in Fig. 19(a). Peak inversion efficiency $> 95\%$ is achieved. An efficiency comparison with stand-alone ($35\text{ W} \leq P_O \leq 70\text{ W}$) and grid-connected ($50\text{ W} \leq P_O \leq 200\text{ W}$) conventional inverters is shown. There is a 7% average improvement in inversion efficiency and about 150 g weight advantage with the SC inverter compared to the stand-alone conventional inverter with similar P_O . The efficiency of a recent PV source fed grid tied conventional flyback inverter [35] that operates in the power range of 50–200 W is also given in Fig. 19(a). This inverter has two power transformers and an output inductor. Fig. 19(b) shows efficiency variation of the proposed inverter with f_s . P_O decreases as f_s is increased due to decrease in $Q_{CT} = C_T \cdot \Delta V_{CT}$ in each cycle. Hence, when f_s is increased, additional SC blocks are needed to deliver the desired P_O . However, the size of C_T and L decreases with increase in f_s . The increase in switching losses and the need for more SC blocks causes a gradual decrease in efficiency with increase in f_s .

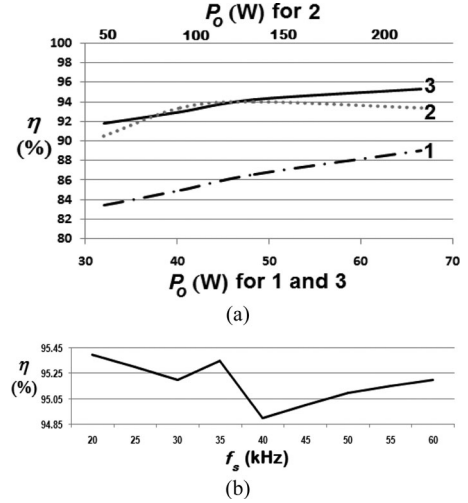


Fig. 19. Inverter Efficiency: (a) Comparison of inversion efficiency with variation in P_O of the proposed SC inverter and conventional inverters. (1) is a conventional stand-alone inverter with $35\text{ W} \leq P_O \leq 70\text{ W}$ (2) is a conventional grid-connected inverter [35] with $50\text{ W} \leq P_O \leq 200\text{ W}$ (3) is the proposed stand-alone SC inverter. (b) Variation of efficiency of the proposed SC inverter with f_s at $P_O \approx 66\text{ W}$.

VII. CONCLUSION AND FUTURE SCOPE

This paper has discussed a SC-based dc–ac inverter with the following features: 1) the inverter is fed from a PV module; 2) it is a single-stage topology for PV module's MPP tracking, output voltage boosting, and inversion, resulting in high efficiency; 3) it has the capability for stand-alone operation since upper limit of output voltage is regulated irrespective of load and intensity of illumination of the PV module; and 4) it has scope for integration with the PV module due to the inherent features of the SC inverter like compactness, ruggedness, and light weight.

A control scheme that utilizes SPWM control and load-dependent output capacitor selection is used to generate a 50 Hz, 110 V pure sine output with a THD $< 4\%$ from a 60 V/70 W PV source. Inversion efficiency $> 95\%$ and tracking efficiency $> 97\%$ are achieved with the hardware model. A mathematical model of the inverter is derived. This is used to formulate a step-by-step method to optimally choose the inverter components. Table II that gives a comparative study of existing SC inverters and converters highlights the uniqueness of the present proposal.

One of the drawbacks of all SC power conditioners is the large number of MOSFET switches needed compared to conventional power conditioners. This drawback may be circumvented if the switches and associated drive circuits are integrated into a single integrated circuit. This will bring out the other relative advantages of SC power conditioners like compactness, ease of manufacturing and ruggedness. Simple heat steering methods described in [4] may be used to minimize the thermal dissipation in this integrated circuit.

The light weight, low height profile and almost constant efficiency over the entire operating range will make this inverter suitable for easy integration with portable unfurlable solar arrays and solar panels mounted on automobiles to enable use of standard 110 V ac appliances while in transit or in remote locations. The proposed SC-inverter-based MPP tracker may be modified for PV-module-integrated grid-connected and per-panel MPP tracking applications [23].

APPENDIX

MATHEMATICAL MODEL OF THE SINGLE-STAGE SC INVERTER TOPOLOGY

Phase 2 (Section IV):

$$v_{C_T/n}(t) = -\frac{1}{C_T/n} \left[\left(\frac{Z_1 e^{r_1 t}}{r_1} \right) + \left(\frac{Z_2 p_1}{p_1^2 + q_1^2} e^{p_1 t} \cos q_1 t + \frac{Z_2 q_1}{p_1^2 + q_1^2} e^{p_1 t} \sin q_1 t \right) + \left(\frac{Z_3 p_1}{p_1^2 + q_1^2} e^{p_1 t} \sin q_1 t - \frac{Z_3 q_1}{p_1^2 + q_1^2} e^{p_1 t} \cos q_1 t \right) \right] \quad (12)$$

$$v_O(t) = -\frac{1}{C_T/n} \left\{ \left(\frac{Z_1 e^{r_1 t}}{r_1} \right) + \left(\frac{Z_2 p_1}{p_1^2 + q_1^2} e^{p_1 t} \cos q_1 t + \frac{Z_2 q_1}{p_1^2 + q_1^2} e^{p_1 t} \sin q_1 t \right) + \left(\frac{Z_3 p_1}{p_1^2 + q_1^2} e^{p_1 t} \sin q_1 t - \frac{Z_3 q_1}{p_1^2 + q_1^2} e^{p_1 t} \cos q_1 t \right) \right\} \\ - (R_{S2} + R_C) Z_1 e^{r_1 t} - Z_2 (R_{S2} + R_C) e^{p_1 t} \cos q_1 t \\ - Z_3 (R_{S2} + R_C) e^{p_1 t} \sin q_1 t - L \\ \left[Z_1 r_1 e^{r_1 t} + Z_2 (p_1 e^{p_1 t} \cos q_1 t - q_1 e^{p_1 t} \sin q_1 t) + Z_3 (p_1 e^{p_1 t} \sin q_1 t + q_1 e^{p_1 t} \cos q_1 t) \right] \quad (13)$$

Phase 3(Section IV):

$$v_O(t) = -L Z_4 p_2 e^{p_2 t} \cos q_2 t + L Z_5 q_2 e^{p_2 t} \sin q_2 t - L Z_5 p_2 e^{p_2 t} \sin q_2 t - L Z_5 q_2 e^{p_2 t} \cos q_2 t \\ - R_C Z_4 e^{p_2 t} \cos q_2 t - R_C Z_5 e^{p_2 t} \sin q_2 t - \frac{R_C V_D}{L C_O R_L} \\ \frac{1}{m_1 m_2} - V_D. \quad (21)$$

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